## REMARKS

The Office Action mailed January 3, 2002, has been received and reviewed. Claims 31 through 35 and 37 through 45 are currently pending in the application. Claims 31 through 35 and 37 through 45 stand rejected. Applicants have amended claims 34 and 35, and respectfully request reconsideration of the application as amended herein.

**35 U.S.C. § 112 Claim Rejections**

Claims 31 through 34, 37 through 41, 44, and 45 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

The Examiner has indicated claims 31 through 34 are indefinite due to confusion with the intended definition of "contiguous". Applicants previously cited a generally accepted definition of "contiguous" in order to highlight distinguishing features of the present invention (see Amendment of October 16, 2001, responding to the Office Action July of 17, 2001). "Contiguous" refers to structures that (1) touch one another, (2) that share a boundary, or (3) that are connected without a break therebetween. *See, e.g.,* The American Heritage College Dictionary, 3d ed. (Houghton, Mifflin 1997). Pointing to Applicants' FIG. 22, the Examiner asserts definitions 1 and 3 are not supported, because mesas or webs exist in FIG. 22 that are separated from other mesas or webs. A review of FIG. 22 shows that while there are some separated mesas or webs, the large majority touch one another or are connected without a break. Claims 31 and 33 recite "A semiconductor capacitor storage poly, *comprising...* " a plurality of contiguous mesas or webs (emphasis added). The transitional term "comprising" is inclusive or open-ended and does not exclude additional, unrecited elements. *See* MPEP §2111.03. Definitions 1 and 3 of "contiguous" accurately describe mesas and webs in Applicants' invention, and separated elements do not render the claim indefinite. Accordingly, Applicants respectfully submit definitions 1, 2, and 3 are supported by the specification.

Regarding claims 37 through 41, 44 and 45, the Examiner asserts a structure having a hemispherical-grain polysilicon layer and a dielectric layer is not supported by the specification because the HSG layer is removed before the dielectric is formed. Applicants respectfully disagree. Contrary to the Examiner's indication that Applicants' FIGS. 7-10 show the HSG layer as being removed, FIG. 8 clearly shows the presence of HSG layer 122. Further, while the disclosure indicates mask layer 124 is removed prior to dielectric deposition, nowhere does it describe removing the remaining HSG layer 122 (see Specification, page 8, lines 19-26).

In view of the foregoing, Applicants respectfully request the withdrawal of the 35 U.S.C. § 112, second paragraph, rejections of claims 31 through 34, 37 through 41, 44, and 45.

**35 U.S.C. § 102(b) Anticipation Rejections**

Anticipation Rejection Based on U.S. Patent No. 5,254,503 to Kenney

Claims 35, 42, and 43 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kenney (U.S. Patent No. 5,254,503). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants respectfully submit Kenney does not describe each and every element of claims 35, 42 and 43. Claim 35, as amended, recites "a contiguous hemispherical-grain polysilicon layer over said storage poly structure". Claim 42 recites "a substantially confluent hemispherical-grain polysilicon layer on said storage poly structure". Claim 43 recites "a mask ... spaced apart from said storage poly structure by said hemispherical-grain polysilicon layer". Kenney does not expressly or inherently describe a contiguous or confluent layer, but rather illustrates discrete islands of hemispherical-grain polysilicon on surface 14 that are etched to

form isolated columns on a storage poly structure 10 (see Figs. 1 and 4). Consequently Kenney also does not describe its mask 16 being spaced apart from the storage poly structure 10 (see Fig. 4). Therefore, Applicants respectfully submit claims 35, 42 and 43 are allowable over Kenney under 35 U.S.C. § 102(b), and request the rejections be withdrawn.

**35 U.S.C. § 103(a) Obviousness Rejections**

Obviousness Rejection Based on U.S. Patent No. 5,358,888 to Ahn et al.

Claims 31 and 32 stand rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Ahn et al. (U.S. Patent No. 5,358,888). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Applicants respectfully submit the 35 U.S.C. § 103(a) obviousness rejections are improper because a *prima facie* case of obviousness has not been made.

Independent claim 31 recites a semiconductor capacitor storage poly that includes downwardly extending recesses and "a plurality of contiguous mesas forming a maze-like structure". Rather than teach a capacitor structure with "contiguous" elements that form a "maze-like" structure, Ahn et al. describes individual islands of the capacitor structure that are laterally isolated from one another (see col. 6, lines 31-64 and Figs. 6 and 16). For this reason, it is submitted that Ahn et al. does not teach or suggest all of the limitations of claim 31.

Regarding obviousness, the Examiner presents no argument for a motivation to add these missing limitations, and there is nothing in the reference or from the knowledge generally available in the prior art which would lead one of ordinary skill to make the modification. Accordingly, Applicants respectfully submit claim 31 is allowable over Ahn et al. under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a), and request the rejection be withdrawn.

Claim 32 is allowable, among other reasons, as depending from claim 31, which is allowable.

Obviousness Rejection Based on U.S. Patent No. 5,358,888 to Ahn et al. in view of U.S. Patent No. 5,254,503 to Kenney

Claims 33, 34, and 38 through 41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahn et al. (U.S. Patent No. 5,358,888) in view of Kenney (U.S. Patent No. 5,254,503). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit the 35 U.S.C. § 103(a) obviousness rejections are improper because a *prima facie* case of obviousness has not been made.

There is no suggestion or motivation in the references or from the knowledge generally available in the prior art which would lead one of ordinary skill in the art to modify Ahn et al. with the teachings of Kenney as has been proposed by the Examiner.

Ahn et al. describes a method for manufacturing a storage poly structure 100 with increased surface area, wherein discrete islands of HSG 80 are deposited on a first material layer 50 for use as an etch mask during formation of recesses in a conductive layer 40 (see col. 6 and Figs. 7-9, 13, 14, 17-19, 23 and 24). The HSG 80 and first material layer are eliminated during etching, and a dielectric and further conductive layer are applied to form a capacitor (see col. 8, lines 29-51).

Kenney teaches a method for forming recesses in a storage poly by forming a mask 16 over irregular features in a surface 14 and etching mask 16 to expose the upper extremities of the

features (see col 4. and Figs. 1-3). The exposed extremities are then etched out to form recesses in storage poly structure 10.

The Examiner submits it would be obvious to combine the references in order to include HSG polysilicon on the top surface of the storage poly 100 of Ahn et al. for the purpose of enhanced surface area and increased capacitance. It is respectfully submitted that this modification would have no such benefit. Ahn et al. uses HSG polysilicon as an etching mask for forming a pattern of recesses within a storage poly. The HSG polysilicon in Kenney is for the entirely different purpose of creating irregular surface features, which are subsequently covered with a mask and etched away. There would be no reason to modify the method of Ahn et al. to add HSG polysilicon in the manner taught by Kenney because after etching, its function as a mask is no longer required. Furthermore, there is nothing in the references or the knowledge generally available in the art that would indicate a reasonable expectation that the modification would successfully provide enhanced surface area and increased capacitance.

Applicants also respectfully submit neither Ahn et al. nor Kenney, alone or in combination, teach or suggest all of the limitations of the rejected claims. Claim 33 recites "a plurality of contiguous webs forming a maze-like structure". Claim 40 recites "said storage poly structure comprises a web-like structure." Ahn et al. and Kenney, on the other hand, describe individual islands that are laterally isolated from one another (see Ahn et al. at col. 6, lines 31-64 and Figs. 6 and 16) and isolated columns on a storage poly structure (see Kenney at Figs. 1 and 4). Claim 38 recites a semiconductor memory cell structure having "regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure ... and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses". Ahn et al. states "The HSG layer 80 is eliminated together with the conductive layer ..." (see col. 8, lines 29-47 and col 10, lines 42-49). Kenney states "Following the transfer of the masked pattern into the substrate, the mask forming layers can be removed and the substrate further processed as necessary" (see col. 4, lines 38-40 and Fig. 6). This indicates the HSG is removed before the addition of dielectric material.

In view of the foregoing, Applicants respectfully submit claims 33, 38 and 40 are allowable over Ahn et al. and Kenney under 35 U.S.C. § 103(a), and request the rejections be withdrawn.

Claims 34, 39 and 41 are allowable, among other reasons, as depending from claims 33 and 38, which are allowable.

Obviousness Rejection Based on U.S. Patent No. 5,254,503 to Kenney

Claims 37 through 39, 41, 44 and 45 stand rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Kenney (U.S. Patent No. 5,254,503). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit the 35 U.S.C. § 103(a) obviousness rejections are improper because a *prima facie* case of obviousness has not been made.

Applicants respectfully submit Kenney fails to describe or teach or suggest all of the limitations of the rejected claims. Claim 37 recites an intermediate semiconductor memory cell structure having "low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure ... and dielectric material at least lining the recesses." Claim 38 recites a semiconductor memory cell structure having "regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure ... and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses". Claim 44 recites an intermediate semiconductor capacitor structure having "a hemispherical-grain polysilicon layer on at least portions of the storage poly structure ... and dielectric material lining at least said recesses." Claim 45 recites an intermediate semiconductor memory cell structure having "a hemispherical-grain polysilicon layer on at least portions of the storage poly structure ... and dielectric material lining at least said recesses."

Kenney, on the other hand, states "Following the transfer of the masked pattern into the substrate, the mask forming layers can be removed and the substrate further processed as

necessary" (see col. 4, lines 38-40 and Fig. 6). As discussed above, this indicates the HSG is removed before the addition of dielectric material. For this reason, it is submitted that Kenney does not teach or suggest all of the limitations of claims 37, 38, 44 and 45.

Regarding obviousness, the Examiner presents no argument for a motivation to add the missing limitation, and there is nothing in the reference or from the knowledge generally available in the prior art which would lead one of ordinary skill to make the modification.

Accordingly, Applicants respectfully submits claims 37, 38, 44 and 45 are allowable over Kenney under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a), and request the rejections be withdrawn.

Claims 39 and 41 are allowable, among other reasons, as depending from claim 38, which is allowable.

## ENTRY OF AMENDMENTS

The amendments to claims 34 and 35 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

## CONCLUSION

Claims 31 through 35 and 37 through 45 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

Brick G. Power
Registration Number 38,581
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

Date: April 1, 2002

BGP/hlg:djp
Enclosure: Version With Markings to Show Changes Made

N:\2269\2914.1\Amendment 2.wpd

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE CLAIMS:**

Please amend the claims as follows:

34. (Amended) The storage poly of claim 33 [31], wherein said webs extend in the X, Y and Z coordinates.

35. (Previously twice amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure with recesses formed therein;

a contiguous hemispherical-grain polysilicon layer over said storage poly structure; and

a mask over said hemispherical-grain polysilicon layer, said recesses being exposed through said contiguous hemispherical-grain polysilicon layer and said mask.